

REMARKS

By the present amendment, the specification has been amended to correct an apparent typographical error. Entry of these amendments is respectfully requested.

In the Office Action, it was required that corrected drawings be submitted. Corrected drawings were filed on November 26, 2002. Accordingly, withdrawal of the requirement is respectfully requested.

An apparent typographical error in the prior Amendment dated August 29, 2002, was noted. As indicated above, the specification has been amended to correct the apparent typographical error.

Claims 1-5 were rejected under 35 USC § 103(a) as being unpatentable over the patent to Morgan et al in view of the patents to Takehara et al and Corbett. Reconsideration of this rejection in view of the following comments is respectfully requested.

With regard to this rejection, it is to be specifically noted that the patent to Takehara et al has a U.S. filing date of November 2, 2000. The subject application has a U.S. filing date of October 12, 2000, prior to the filing date of the cited patent. Thus, the Takehara et al patent is not effective prior art to the subject application under 35 USC § 103(a) or (e).

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For the reasons stated above, withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claim 1 through 5 over the cited patents are respectfully requested.

In view of the foregoing, it is submitted that the subject application is now in condition for allowance and early notice to that effect is earnestly solicited.

In the event this paper is not timely filed, the undersigned hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 01-2340, along with any other additional fees which may be required with respect to this paper.

Respectfully submitted,

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Marked Up Version of Amendments to Specification and Claims

IN THE SPECIFICATION:

Amend the specification as follows:

(Page 13, lines 1-26):

thereafter attach the resin sheet having the marking to the rear surface of the wafer.

Thereby, the marking information including the position information and result of electrical test is not required to temporarily print unlike the first embodiment and the result of electrical test can be marked on the resin sheet simultaneously when the test is performed.

Moreover, it is also possible to previously print the numerals and codes indicating the position information of the chip on the resin sheet and then attaching the resin sheet to the rear surface of wafer under the condition of Fig.2(a). In this case, the result of electrical test is not printed. The result of electrical test is no longer required to print on the resin sheet in the case where such result is stored in the memory together with the position information of chip. Thereby, the marking process of the test result may be omitted and accordingly the processes may be saved.

[Effect of the Invention]

As explained above, according to the method of manufacturing wafer level semiconductor device of the present invention, sine since the information indicating where the internal chips are located on the wafer can be printed on the diced semiconductor package, the trace-ability of search for defective product can be very much improved.